REMARKS

Claims 1, 4-15, and 18-19 are pending in the present application. Claims 1 was rejected under 35 U.S.C. §102, as anticipated by U.S. Patent Application Publication No. 2002/0042909 (Van Gageldonk, *et al.*), and claims 4-9, 15 and 18-19 were rejected under 35 U.S.C. §103 as obvious over Van Gageldonk in view of U.S. Patent Application Publication No. 2001/0004755 (Levy, *et al.*). In addition, claims 10-11 were rejected under 35 U.S.C. §102, as anticipated by U.S. Patent Application Publication No. 2001/0042190 (Tremblay, *et al.*), and claims 12-14 were rejected under 35 U.S.C. §103 as obvious over Tremblay in view of Levy. Applicant has amended claim 1. No new matter has been introduced.

Applicant urges that claim 1 is not anticipated by Van Gageldonk for at least the reasons presented below.

At the very least, Van Gageldonk does not disclose or suggest a microprocessor for processing instructions that includes *a plurality of register sub-files . . . wherein the register sub-files each have a same number of registers,* and *wherein each of the clusters is associated with corresponding one of the register sub-files, and each of the register sub-files is associated with a corresponding one of the clusters,* as essentially recited in claim 1.

Van Gageldonk's FIG. 1 and paragraph [0025] disclose functional unit clusters UC1 and UC2 as sharing register file RF1, functional unit clusters UC3 and UC4 as sharing register file RF2, and functional unit clusters UC5 and UC6 as sharing register file RF3. Thus, although each functional unit is associated with a single register file, each register file can be associated with more than one functional unit, contrary to the recitation of Applicant's claim 1.

Furthermore, the Examiner cites Van Gageldonk's FIG. 1 as disclosing that register files RF1 and RF2 have a same number of registers. Applicant urges that nothing can be inferred regarding the number of registers in a register file from the blocks in the figure that represent the register files. Van Gageldonk's FIG. 1 depicts blocks of different sizes representing the register files, which suggests that Van Gageldonk's register sub-files can have a different number of registers. In addition, the section of Van Gageldonk that describes the register files, paragraph [0025], discloses nothing regarding the number of registers in each register sub-file. Paragraph [0025] instead describes how the functional units are connected to the register sub-files, and how the physical registers can be organized within the register sub-file. Applicant urges that the Examiner is incorrect in stating that Van Gageldonk discloses register sub-files having a same number of registers.

Thus, for the reasons presented above, Applicant urges that Van Gageldonk does not anticipate claim 1. Reconsideration and withdrawal of this section 102 rejection are respectfully requested.

Applicant urges that claim 10 is not anticipated by Tremblay for at least the reasons presented below.

At the very least, Tremblay does not disclose or suggest a microprocessor for processing instructions that includes *a plurality of register files . . . wherein each of the plurality of register files has at least one read port from which any of the plurality of clusters can read data.*

The processor disclosed in Tremblay includes a plurality of functional units and a multi-ported register file that is divided into a plurality of register segments, wherein each register segment is associated with one functional unit. Each register segment is partitioned into local registers and global registers. Although the global registers can be read from and written to by all functional units, the local registers can be read from and written to by only the functional unit associated with the particular register file segment. Thus, Tremblay

includes register segments that cannot be read by any of the plurality clusters, contrary to the recitation of claim 10.

Since Tremblay does not disclose all of the limitations of Applicant's claim 10, Tremblay does not anticipate claim 10. Reconsideration and withdrawal of this section 102 rejection are respectfully requested.

Claim 11 depends from claim 10, and is thus patentable for at least the same reasons as claim 10. Reconsideration and withdrawal of this section 102 rejection are respectfully requested.

Claims 4-9 depend from claim 1, and claims 12-14 depend from claim 10. The Action cited Levy as disclosing a register-renaming unit as recited in claims 4 and 12. However, although Levy discloses functional units and register files, Levy does not disclose the *register sub-files [that] have a same number of registers,* as recited in claim 1. Thus, Applicant urges that Levy does not correct for the deficiencies of Van Gageldonk. Therefore, Applicant urges that a *prima facie* case of obviousness of claims 4-9 cannot be maintained over Van Gageldonk and Levy. Furthermore, Levy does not disclose *a plurality of clusters* and *a plurality of register files . . . wherein each of the plurality of register files has at least one read port from which any of the plurality of clusters can read data.* Thus, Applicant urges that Levy does not correct for the deficiencies of Tremblay. Therefore, Applicant urges that a *prima facie* case of obviousness of claims 12-14 cannot be maintained over Tremblay and Levy. Reconsideration and withdrawal of these rejections are respectfully requested.

Applicant urges that claim 15 is not obvious over Van Gageldonk in view of Levy for at least the reasons presented below.

As stated above, Van Gageldonk does not disclose or suggest a method of processing instructions in a microprocessor that includes *a plurality of register sub-files each having a plurality of registers for storing data for executing the instructions, wherein the register sub-files each have a same number of registers,* as essentially recited in claim 15. Furthermore, as stated above, Van Gageldonk does not disclose or suggest a method of processing instructions in a microprocessor that includes *associating each of the register sub-files with corresponding one of the clusters.* The Examiner cited Levy for disclosing renaming target registers in the instruction with registers in a register sub-file. However, although Levy discloses floating point registers and integer registers, Levy does not disclose the *register sub-files each have a same number of registers*, nor does Levy disclose *providing clusters* and *associating each of the register sub-files with corresponding one of the clusters,* and thus Levy does not rectify the deficiencies of Van Gageldonk.

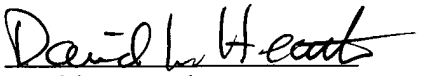
Thus, Applicant urges that a *prima facie* case of obviousness of claim 15 over Van Gageldonk and Levy cannot be maintained. Reconsideration and withdrawal of this section 103 rejection are respectfully requested.

Claims 18-19 depend from claim 15, and are thus patentable for at least the same reasons as claim 15. Reconsideration and withdrawal of these rejections are respectfully requested.

CONCLUSION

Applicant urges that claims 1, 4-15, and 18-19 are in condition for allowance for at least the reasons stated. Early and favorable action on this case is respectfully requested.

Respectfully submitted,

By: 

David L. Heath
Reg. No. 46,763
Attorney for Applicant

Mailing Address:

F. Chau & Associates, LLC
130 Woodbury Road
Woodbury NY 11797
(516) 692-8888
(516) 692-8889 (FAX)